THREE-DIMENSIONAL MMIC TECHNOLOGY FOR MULTIFUNCTION INTEGRATION AND ITS POSSIBLE APPLICATION TO MASTERSLICE MMIC

Tsuneo Tokumitsu, Kenjiro Nishikawa, Kenji Kamogawa,
Ichihiko Toyoda, and Masayoshi Aikawa

NTT Wireless Systems Laboratories
1-2356 Take, Yokosuka-shi, Kanagawa 238-03, Japan

ABSTRACT

We first verified that the integration level of multifunction MMIC's can be easily increased three-fold by using three-dimensional (3-D) MMIC structure, in comparison to planar ones. The technology was used to build high-density masterslice MMIC's on a single footprint in 2 x 2 mm by incorporating two levels of ground metals in the 3-D structure.

INTRODUCTION

Many single-chip receiver/transmitter MMIC's have been fabricated recently in planar forms[1] to cover IMS, DBS, and higher frequency bands reaching into the V band. However, the integration level, *I*, defined as the gain (G in dB)-band width ($\Delta f/f_0$) product per mm^2, decreases along a curve of $I \times f^{1/2}$ (GHz) = 2 (I < 0.9 above 5 GHz). Employing the three-dimensional MMIC's shown in Fig. 1, which use thin polyimide-film layers on GaAs wafers, is an effective way to significantly increase *I* [2]-[5].

We first verified that the largest *I* reaches 2 in the X band and 1.7 in the K band, that is to say, a threefold increase in comparison to planar ones. The reasons for this are that passive circuits have a narrow line-width and spacing of less than 30 µm due to the four polyimide layers, which are as thin as 2.5 µm each, and that these circuits are stacked in the upper and lower levels of the polyimide layers. The implementation of receivers was also supported by a miniature-amplifier topology that achieves a reasonable gain and bandwidth even when using narrow and lossy lines. The three-dimensional MMIC technology was further expanded to advanced masterslice MMIC's on a single footprint by introducing two levels of ground metals in the structure. This technology offers effective elimination of the semiconductor device process and the mask set for the process, as well as a high integration level, resulting in a much shorter turn-around-time and lower cost.

MINIATURIZATION OF AMPLIFIERS

The miniaturization of amplifiers is a key issue in high-density single-chip receiver implementation. A cascode FET, which connects a common-source FET and a common-gate FET with a nearly 2-mm-long TFMS line for the X band, is successfully used for the gain block. Since the intermediate TFMS line significantly modifies and enlarges the S parameters for the cascode connection, the length was adjusted for the designed frequency band and the effect was used to minimize the matching circuit area and to compensate the loss.

Relatively wideband, 10-12.5 GHz, 8-dB gain amplifiers fabricated using the three-dimensional MMIC structure and 0.3-µm-gate-length MESFET's are shown in Figs. 2 (a) and (b). The amplifier in Fig. 2 (a) has input and output matching circuits stacked above and below a ground metal in the middle of the layers. The amplifier in Fig. 2 (b) employs two levels of ground metals and three array-units arranged side-by-side on

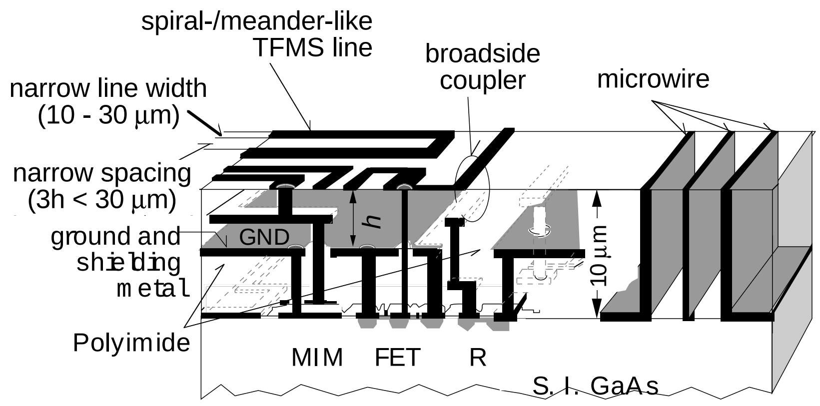


Fig. 1 Basic structure of the three-dimensional MMIC. The left side is focused on in this report.

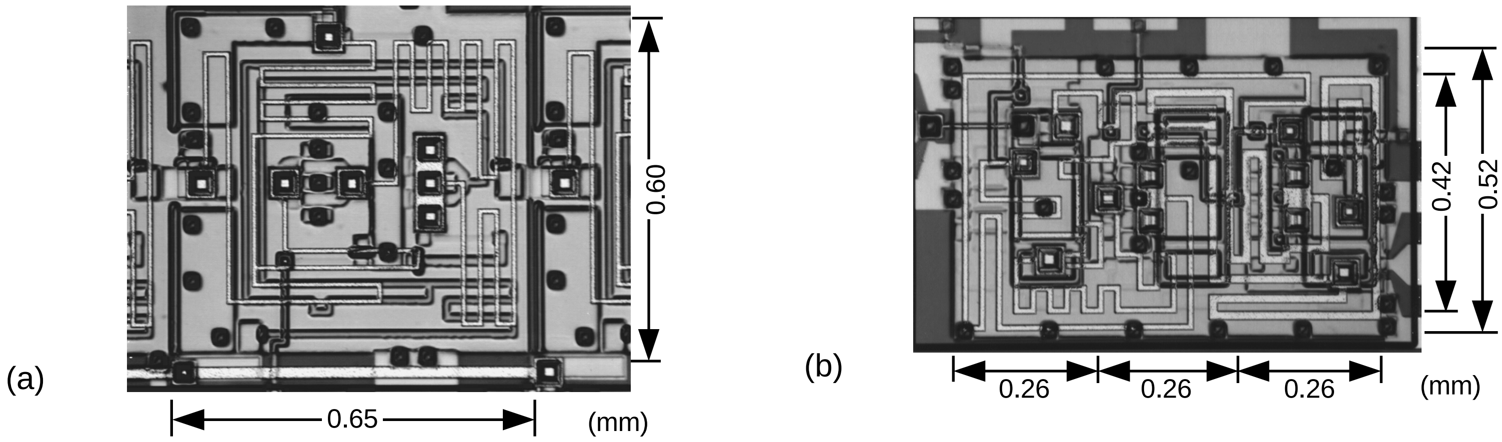


Fig. 2 Miniaturized 3-D MMIC amplifiers with a reasonable gain and bandwidth

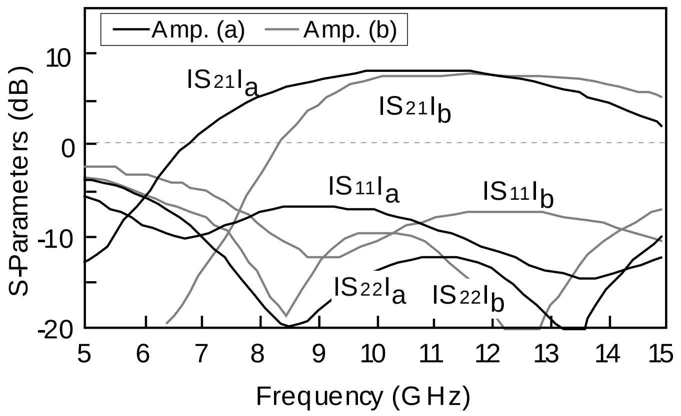


Fig. 3 Performance of 10-12.5 GHz amplifiers (a) and (b)

the wafer surface: each unit consists of a 200-μm-gate-width FET, lower electrodes for MIM capacitors, and resistors in a 0.26 x 0.42 mm area. The gain-frequency characteristics for both amplifiers are shown in Fig. 3. The areas occupied by the amplifiers are 0.65 x 0.60 mm and 0.78 x 0.52 mm, i.e., only 0.4 mm^2. A 16.5-21.5 GHz, 8-dB gain amplifier with stacked matching circuitry is also shown in Fig. 4, which area is 0.55 x 0.50 mm, i.e., less than 0.3 mm^2. Above this frequency the stacked structure is not always used to employ lower-loss TFMS lines associated with 10-μm-thick polyimide substrate.

The 0.4 mm^2 area can be maintained for amplifiers above 5 GHz. Verification of the 3-D amplifier design in various frequency bands and gains is shown in Fig. 5 (measured). Four-stage X- and K-band amplifier chains exhibited a gain of 30 dB with an area of 1.4 mm^2. Therefore, the three-dimensional amplifiers stay along a gain (G)-area (S) curve of G = 21S, while conventional reactive-matching planar ones are within G =4S and G=10S, or 6.5S on avearage [1].

SINGLE-CHIP INTEGRATION OF RECEIVERS

Miniaturization of amplifiers and mixers, as well as passive circuits such as dividers and couplers[4], was performed in the three-dimensional structure. The areas of the functions stay around 0.4 mm^2 over a very wide frequency range; the passive functions do not exceed

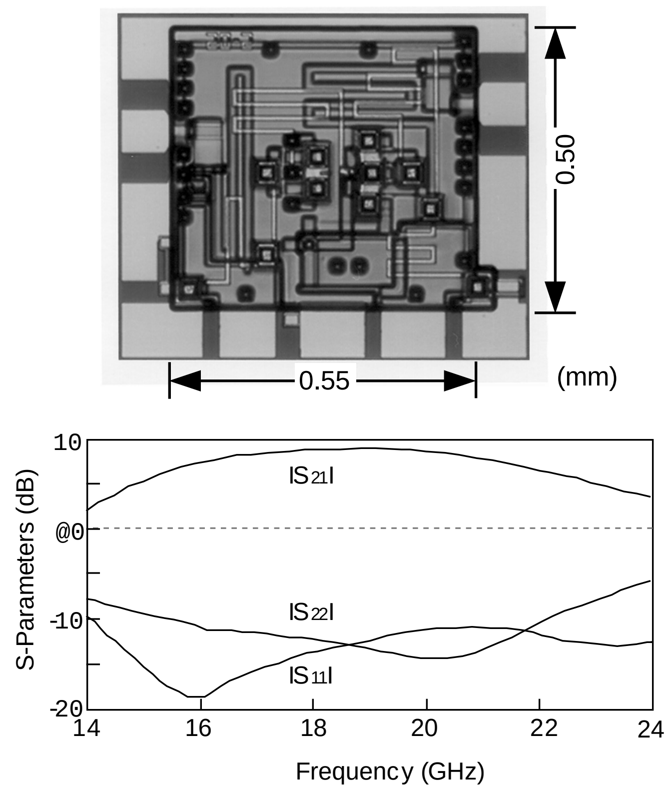


Fig. 4 A miniaturized 20-GHz-band amplifier and the performance

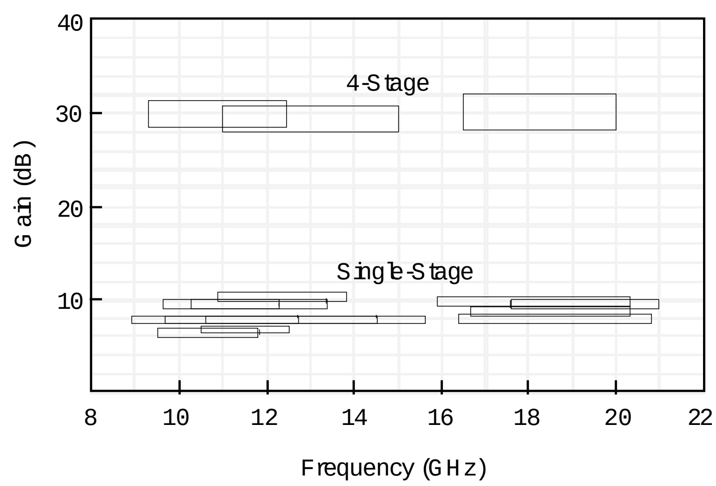


Fig. 5 3-D MMIC amplifiers in various frequency bands (measured)

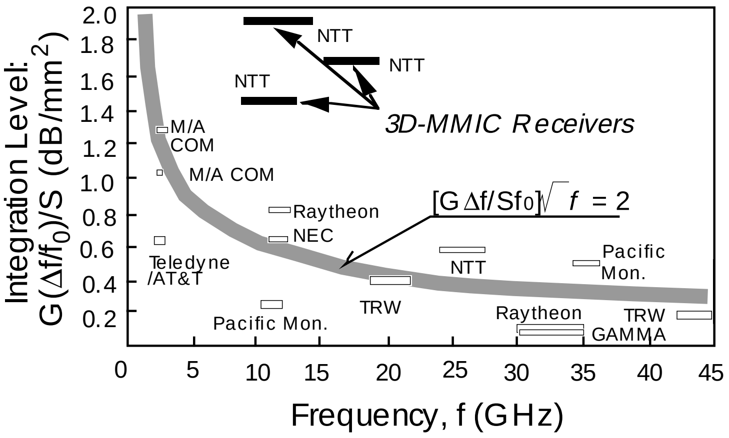


Fig. 6 A comparison of integration level, *I*, defined as gain (dB)-bandwidth (%) product per mm^2.

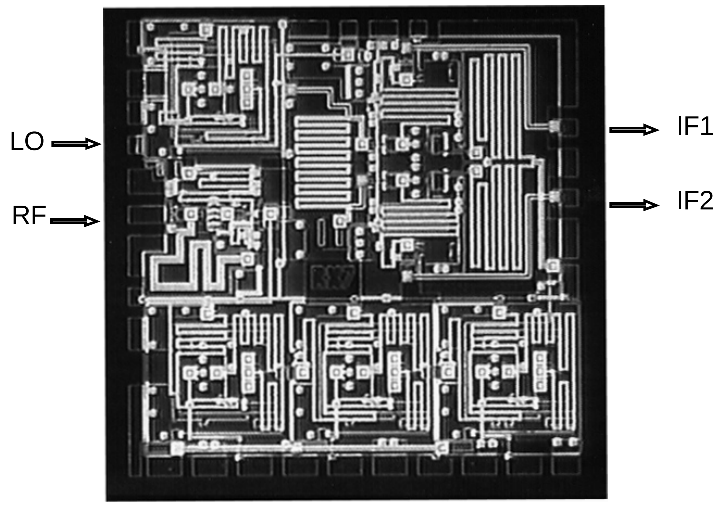
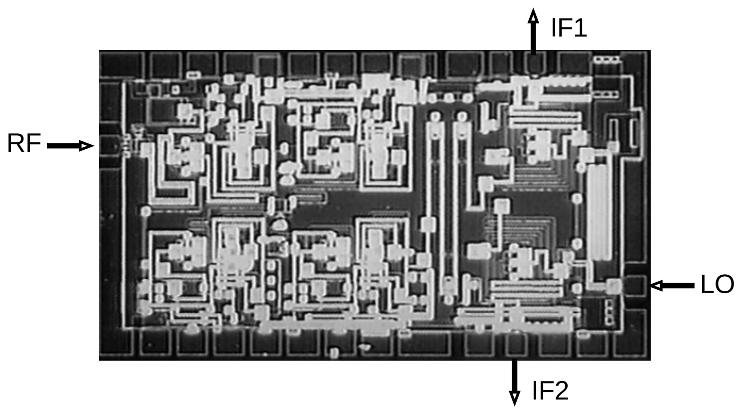


Fig. 7 X-band receiver MMIC (2 x 2 mm)

the average area because of the meander-like or spiral-like, and stacked configurations. This significantly advances the single-chip integration of receivers and transmitters. Figure 6 compares the integration level, *I*, between the three-dimensional and conventional planar receivers.

Fabricated X-[7] and K- band receiver MMIC's are shown in Figs. 7 and 8. The 3D-MMIC receivers contain a low-noise amplifier and a three-stage gain block for the front-end amplification, an image-rejection mixer with a pair of single-mixers, a Wilkinson divider, a 90-degree broadside coupler, and a local amplifier. The functions are integrated in an area of 4 mm^2 and 2.6 mm^2, respectively, with a gain and image-rejection ratio of greater than 20 dB, and an operating-frequency band of around 25 %. The noise figure of the X-band receiver measures 6 dB. A threefold increase in the integration level was achieved with no electro-magnetic coupling between line-segments because of using the very thin polyimide films as substrate.



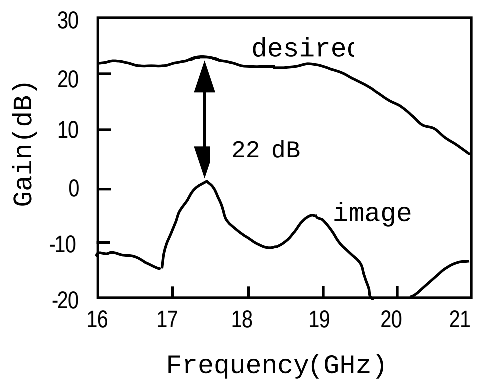


Fig. 8 K-band receiver MMIC (2.2 x 1.2 mm)

MASTERSICE MMIC

The three-dimensional MMIC technology presents a promising way to build masterslice MMIC's on GaAs and Si [6]. The novel masterslice MMIC structure shown in Fig. 9 expands the advantages of the three-dimensional MMIC. Many units, each of which contains transistors, resistors, and lower electrodes for MIM capacitors, are located repeatedly (nearly 6 units/mm^2) on a GaAs or Si wafer to form a master array, and the entire surface is passivated. The on-wafer elements, which are not selected for microwave circuit design, are covered with a ground metal, GND1. Both thin polyimide layers and an additional ground metal, GND2, are stacked over the wafer and GND1 to complete the three-dimensional MMIC design. Therefore, a space for many miniature passive circuits is created over GND1, where the upper electrodes of MIM capacitors are used for GND1 in order to maximize the space. GND1 and the polyimide film layers provide passive circuits independent of the substrate properties (semi-insulating or conductive).

X-band and K-band, single-chip receiver MMIC's were designed and fabricated in a 2 x 2 mm GaAs die, using the masterslice MMIC design rule. Figure 10 shows masterslice MMIC implementation on 6 x 3 units arrayed in an area of 1.8 x 1.8 mm. Fig. 10 (b) is an X-band receiver. A three-stage variable-gain amplifier is located in the left half, an image-rejection mixer on the lower side of the right half, and there is unused space in

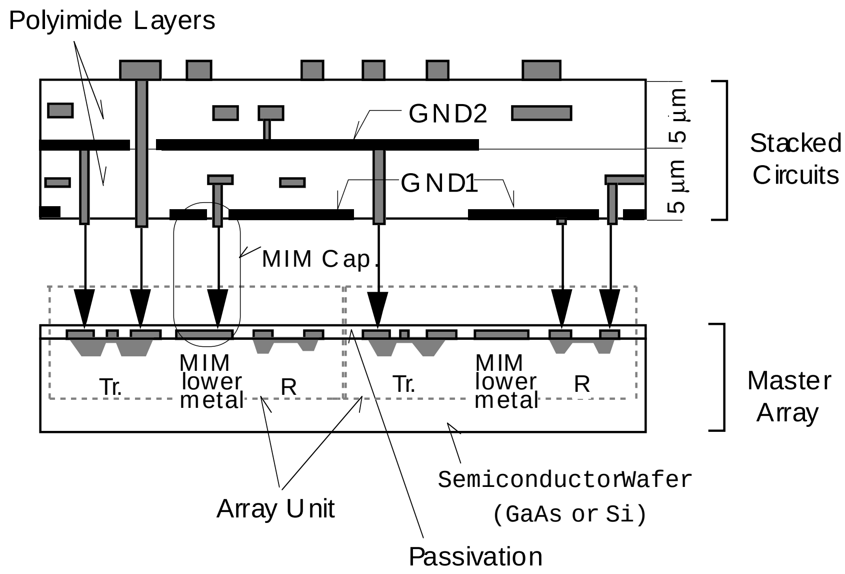


Fig. 9 A masterslice MMIC structure using the 3-D MMIC technology

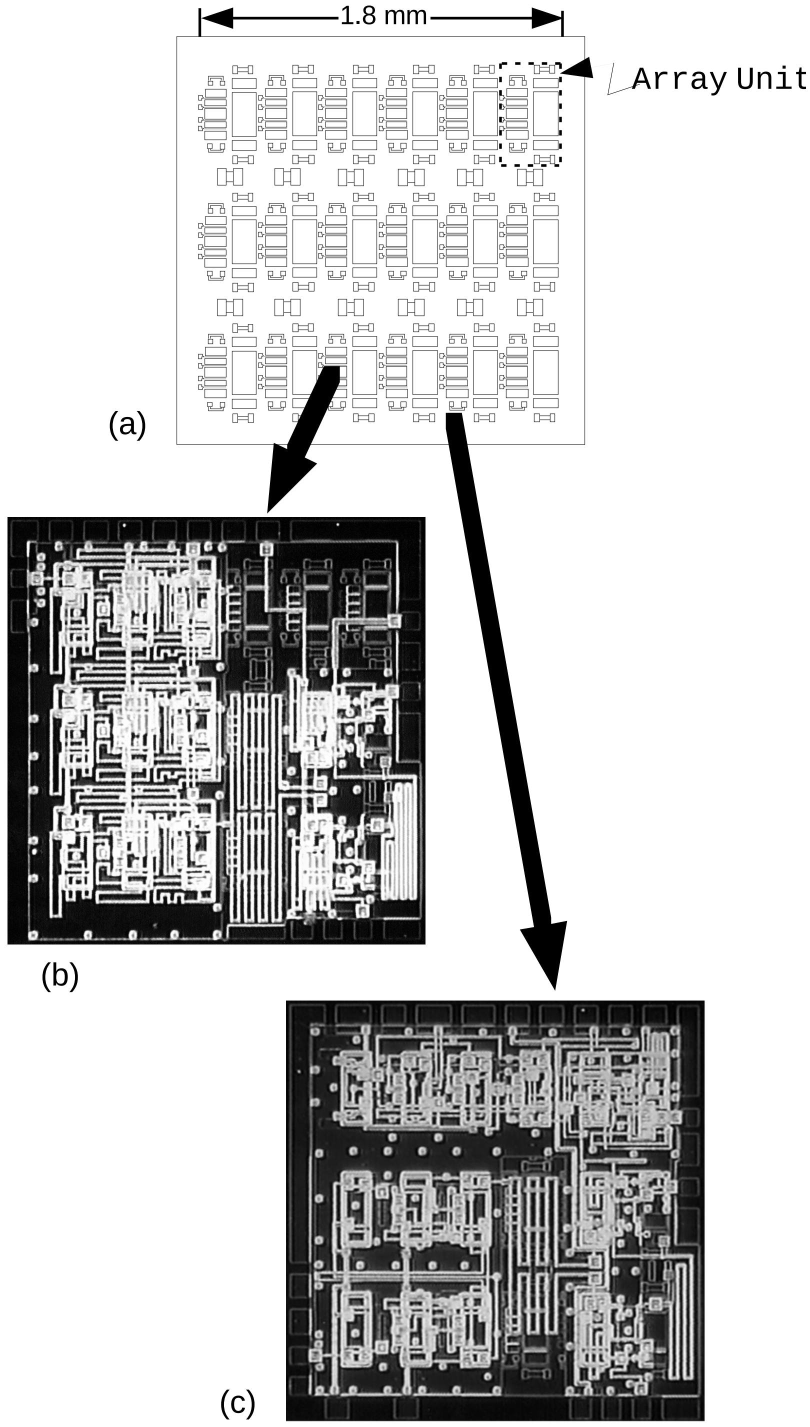


Fig. 10 Masterslice MMIC's; (b) and (c), fabricated on a single footprint, (a), with 6 x 3 master-array units

the upper portion of the right half. A portion of array shows through the unused area in GND2. Fig. 10 (c), which contains an injection-locked oscillator[8] in the upper portion, is designed for 20-GHz-band operation.

CONCLUSION

A threefold integration-ratio increase with three-dimensional MMIC technology has been demonstrated experimentaly. The 3-D MMIC technology is further effective for an accurate design of high-density millimeter-wave MMIC's due to the narrow line width and spacing. Also presented was a novel masterslice MMIC concept, that promises cost-effective production and a quick response to rapidly changing GaAs and Si MMIC markets.

Finally, the authors would like to thank Dr. Kenji Kohiyama, Dr. Kazuo Hirata, Dr. Kimiyosi Yamasaki, and Dr. Makoto Hirano of NTT Wireless Systems Labs. and NTT LSI Labs. for their helpful discussions.

REFERENCES

[1] Proceedinds *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium* from 1988 to 1994.

[2] T. Tokumitsu et al., "Multilayer MMIC using a 3 µm x 3-layer dielectric film structure," in Proc. *IEEE MTT-S Int. Microwave Symp.*, May 1990, pp.831-834.

[3] S. Banba et al., "Small-sized MMIC amplifiers using thin dielectric layers," *IEEE Trans. Microwave Theory Tech.*, Vol. MTT-43, No. 3, pp. 485-492, March 1995.

[4] I. Toyoda et al., "Multilayer MMIC branch-line coupler and broadside coupler," in Proc. *IEEE MTT-S Int. Microwave Symp.*, June 1992, pp. 79-82.

[5] M. Hirano et al., "Three-dimensional passive circuit technology for ultra-compact MMICs," in Proc. *IEEE Int. Microwave Symp.*, May 1995, pp. 1447-1450.

[6] T. Tokumitsu et al., "Three-dimensional MMIC @ technology: Possible solution to masterslice MMIC's on GaAs and Si," *IEEE Microwave and Guided Wave Letters*, Vol. 5, No. 11, pp. 411-413, Nov. 1995.

[7] I. Toyoda et al., "Highly integrated three-dimensional MMIC single-chip receiver and transmitter," in Proc. *IEEE International Microwave Symposium*, June 1996, TH1A-1.

[8] T. Tokumitsu et al, "A novel injection-locked oscillator MMIC with combined ultrawide-band active combiner /divider and amplifiers," *IEEE Trans. Microwave Theory Tech.*, Vol. 42, No. 12, pp.2572-2578, Dec. 1994.